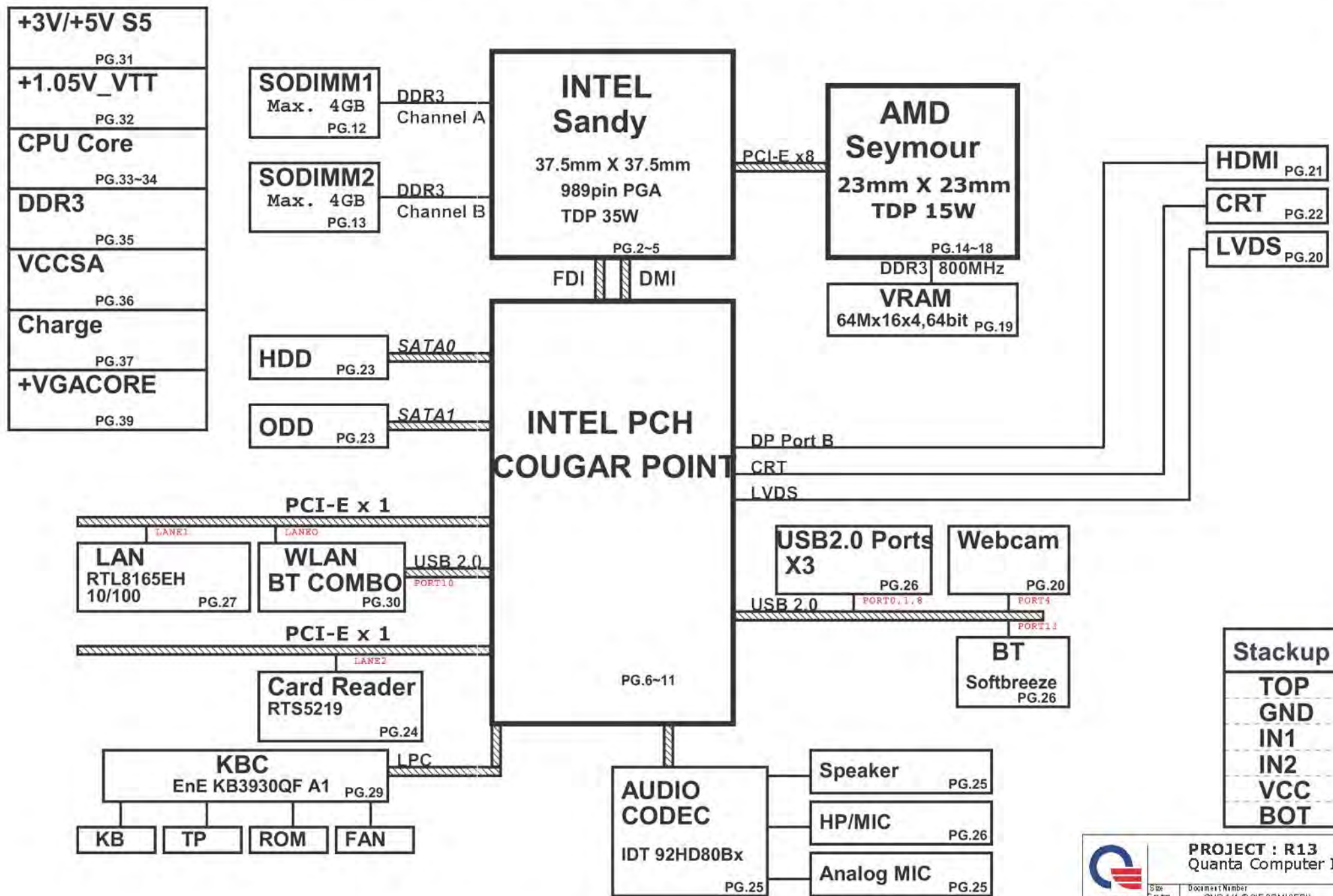
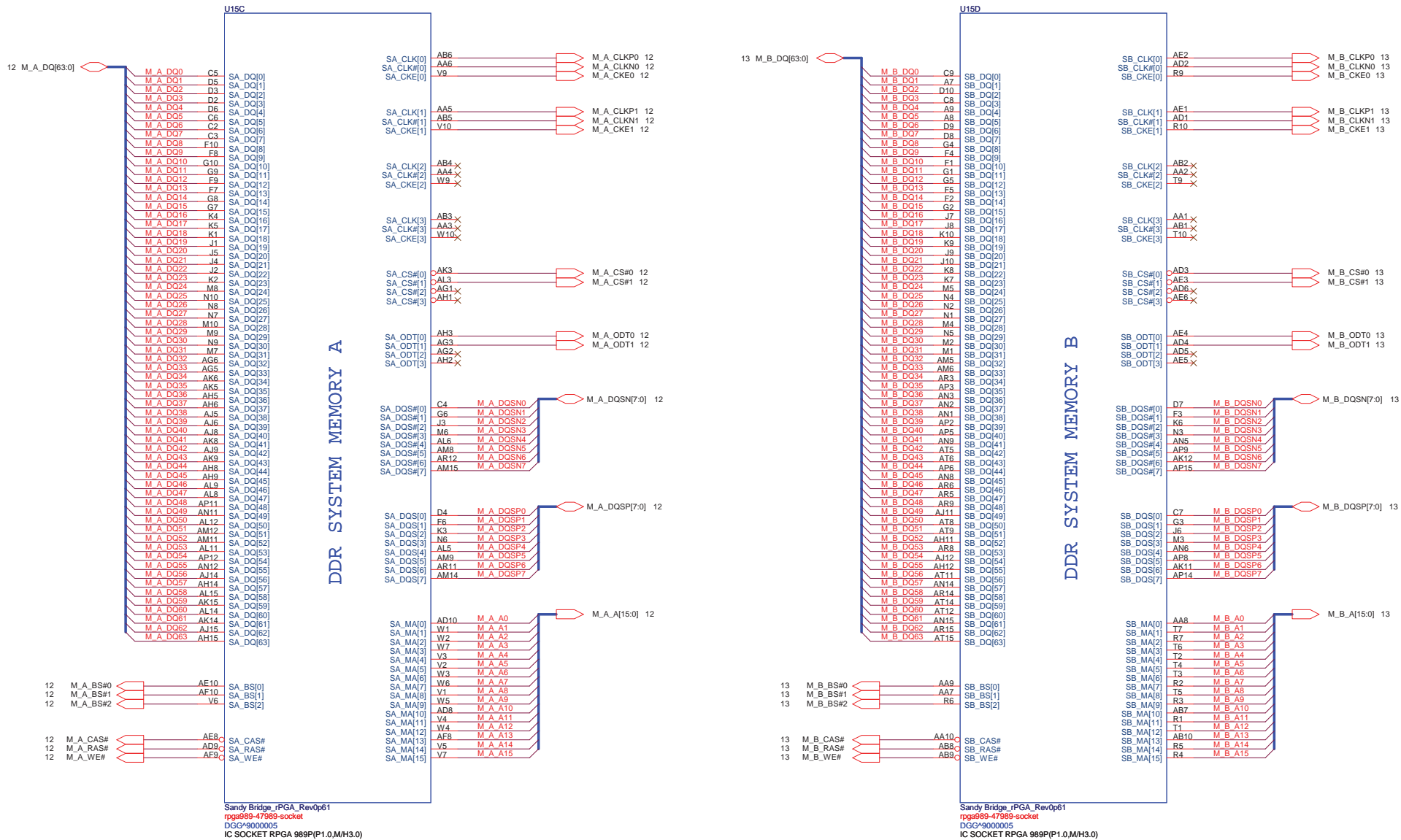


R13 INTEL UMA/DISCRETE SYSTEM DIAGRAM

01




Sandy Bridge Processor (DDR3)

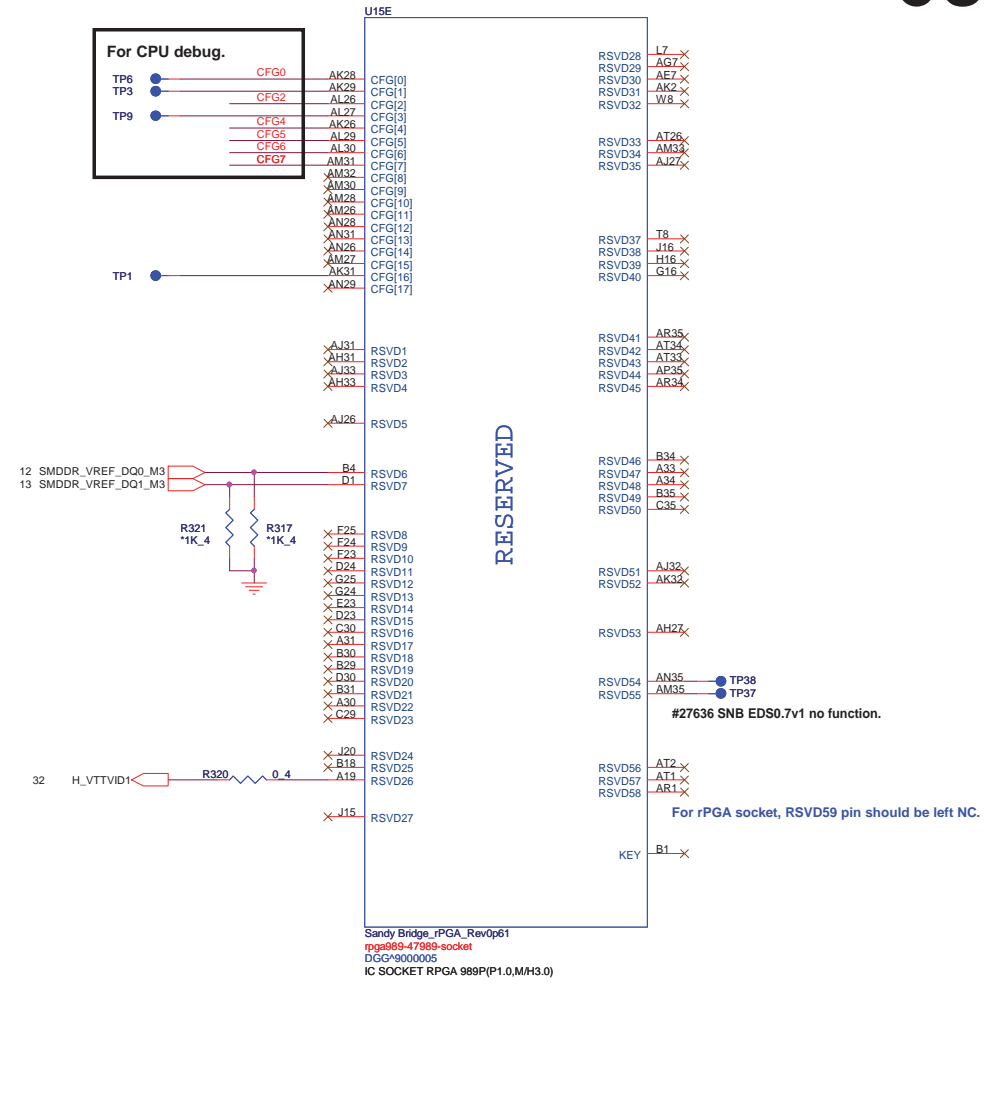



Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

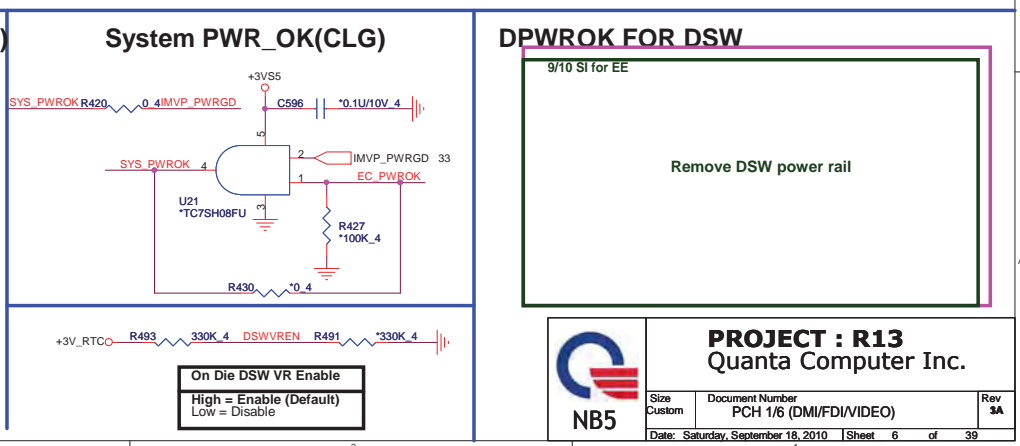
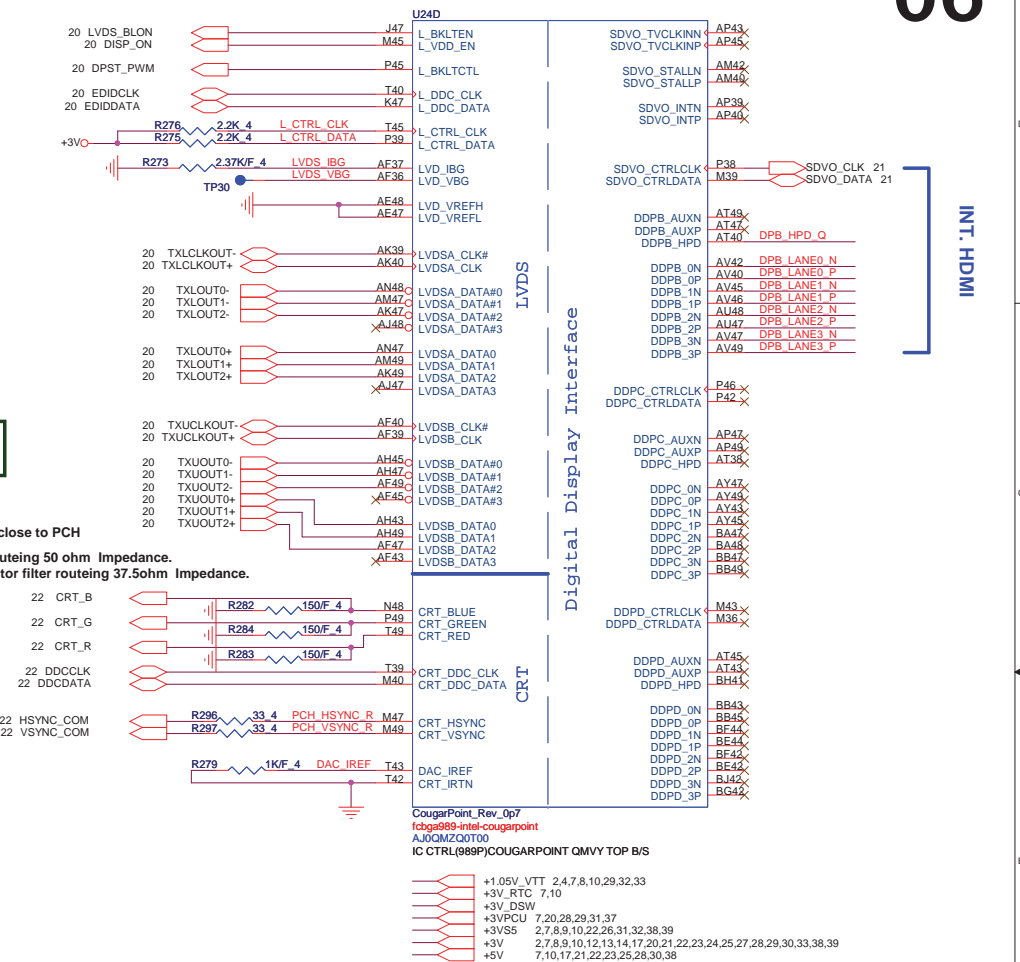
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000005
IC SOCKET RPGA 989P(P1.0,M/H3.0)

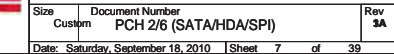
	PROJECT : R13 Quanta Computer Inc.	
	Size Custom	Document Number SNB 2/4 (DDR3 I/F)
	Rev 3A	
Date: Saturday, September 18, 2010 Sheet 3 of 39		



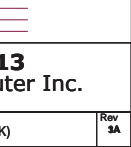
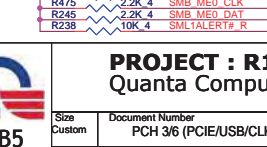
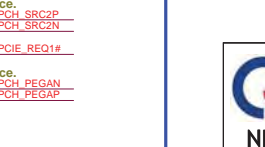
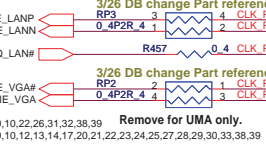
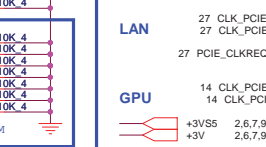
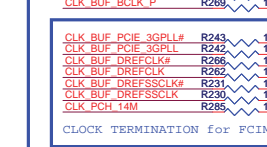
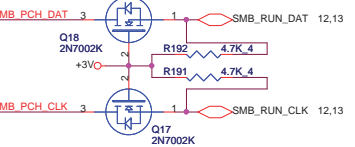
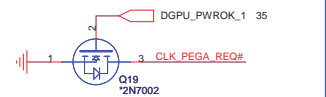
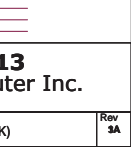
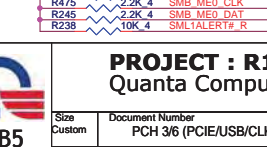
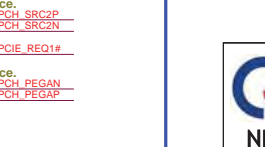
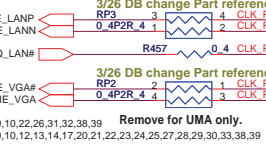
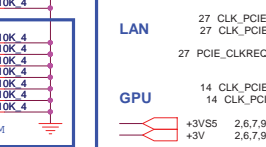
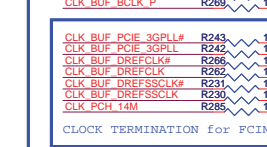
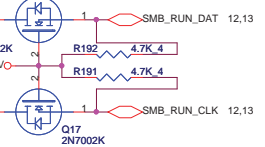
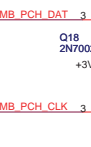
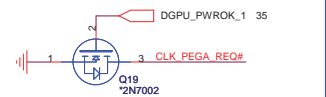


 NB5	PROJECT : R13 Quanta Computer Inc.		
	Size Custom	Document Number SNB 4/4 (GND)	Rev 3A
	Date: Saturday, September 18, 2010	Sheet 5 of 39	





U24E



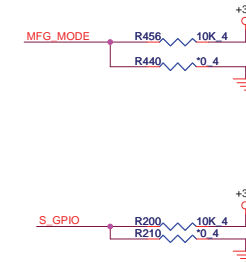
Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

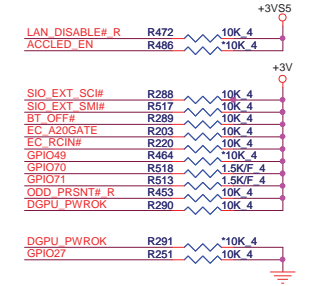
09



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

SV_SET_UP
High = Strong (Default)

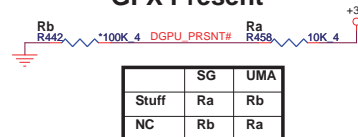
TEST DETECT
Low = Default

9/3 SI for H/W.

DMI TERMINATION VOLTAGE OVERRIDE Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

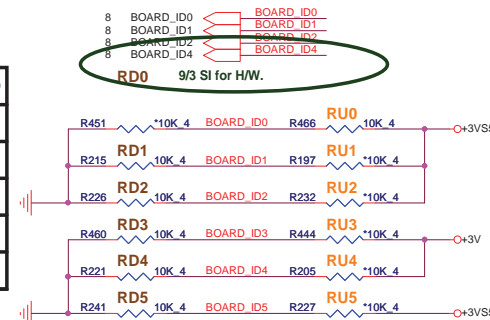
FDI TERMINATION VOLTAGE OVERRIDE LOW - Tx, Rx terminated to same voltage

GFX Present



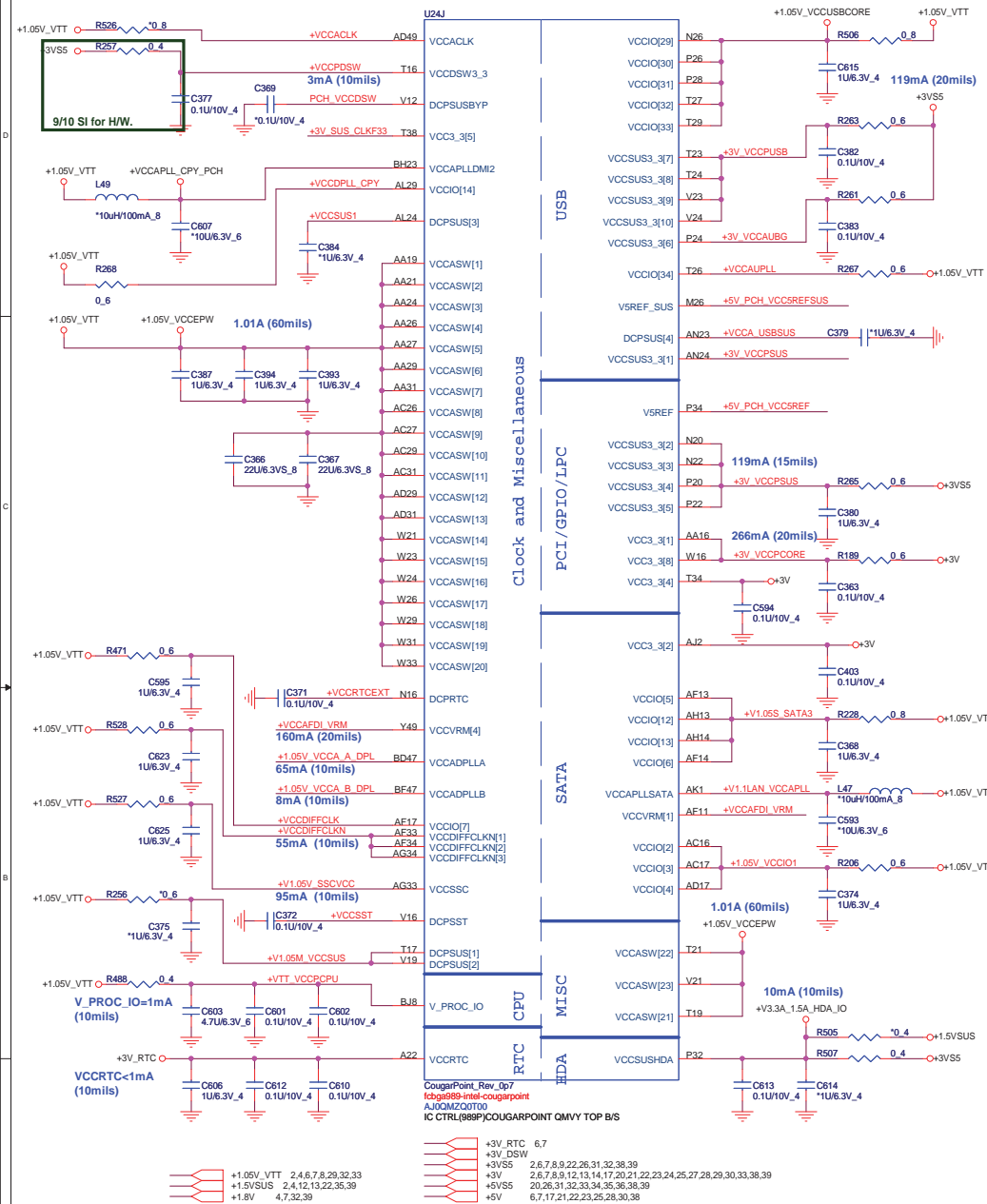
BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
	0	0	0	0	0	0
	0	0	0	0	0	0
	0	0	0	0	0	0

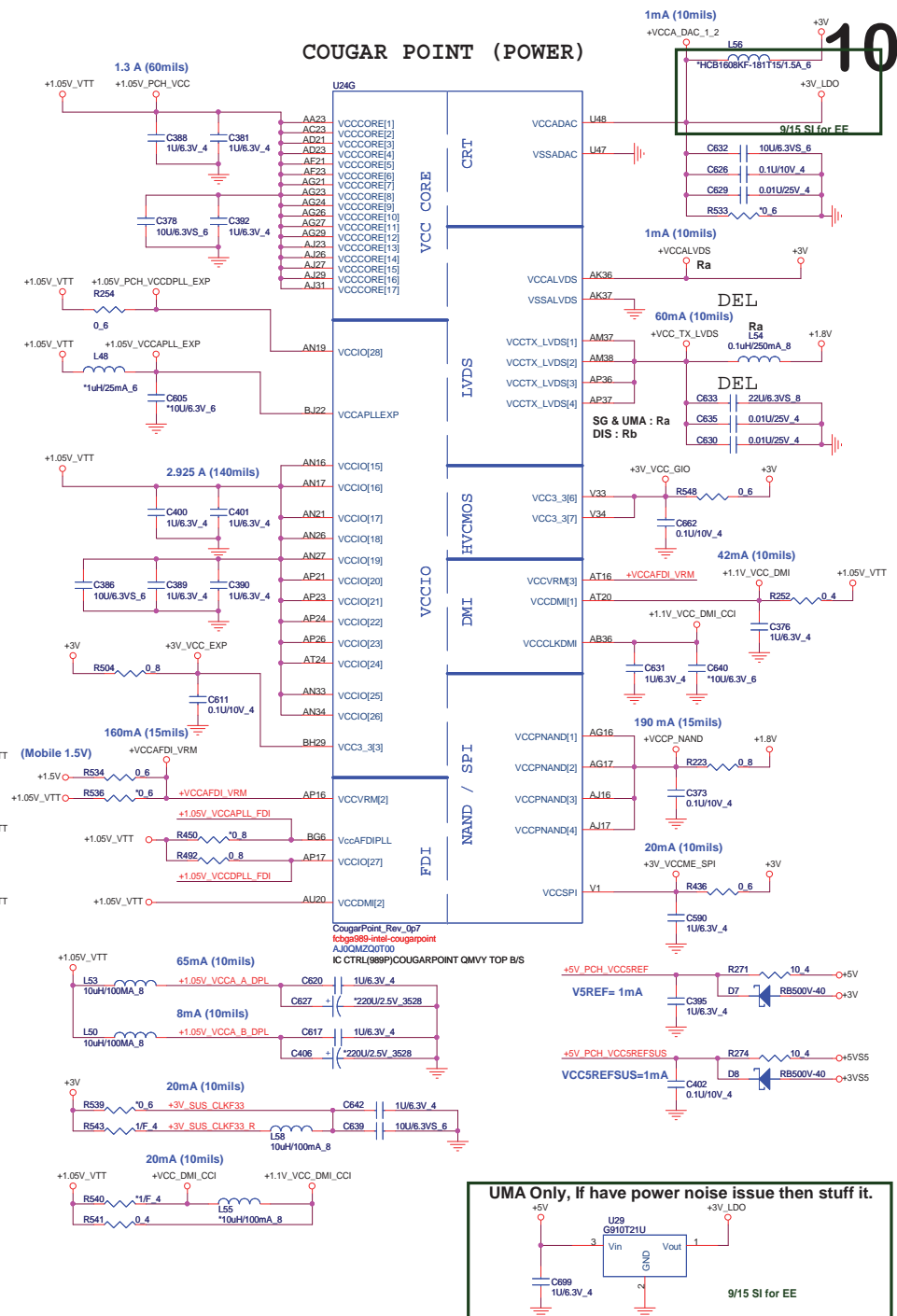


PROJECT : R13
Quanta Computer Inc.

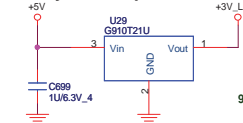
Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 3A
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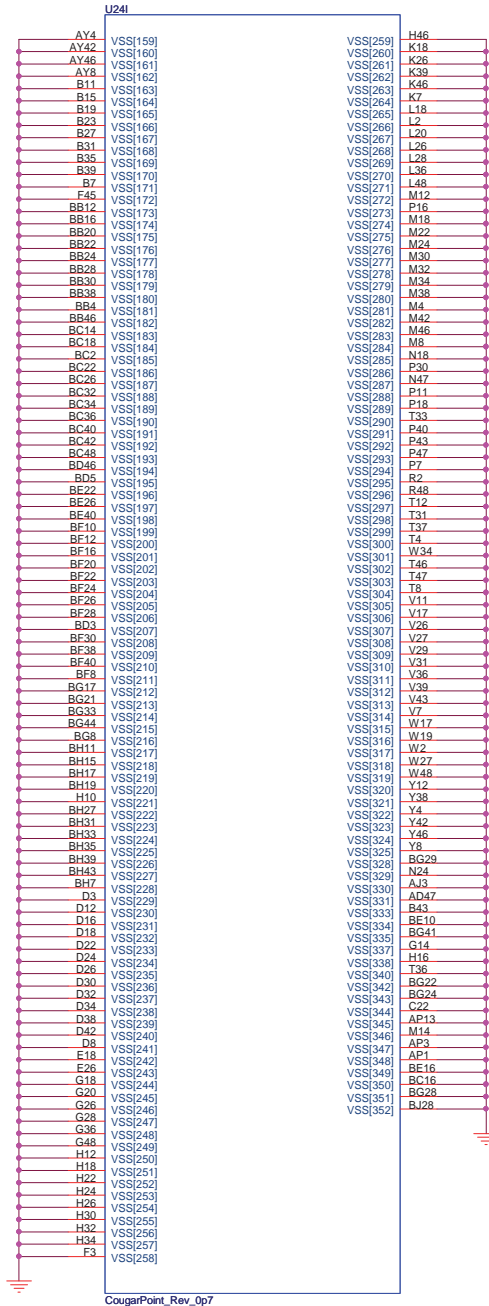
COUGAR POINT (POWER)



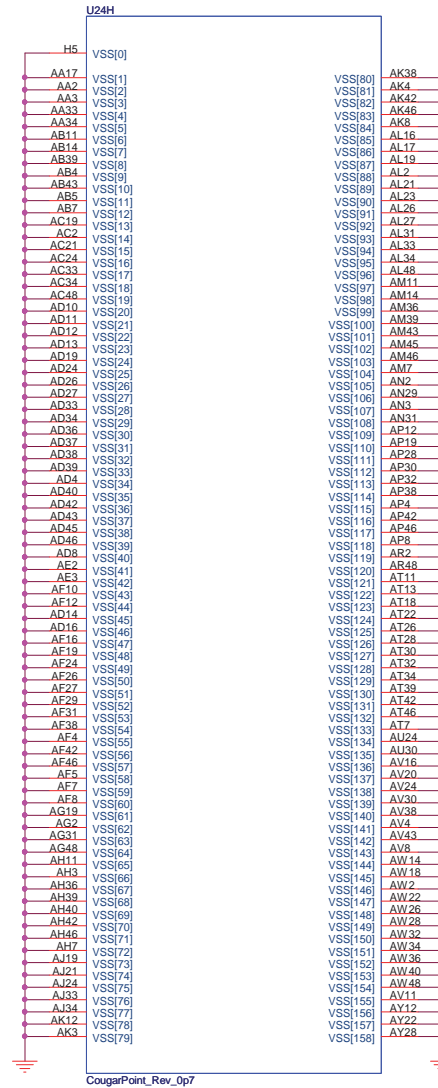
UMA Only, If have power noise issue then stuff it.

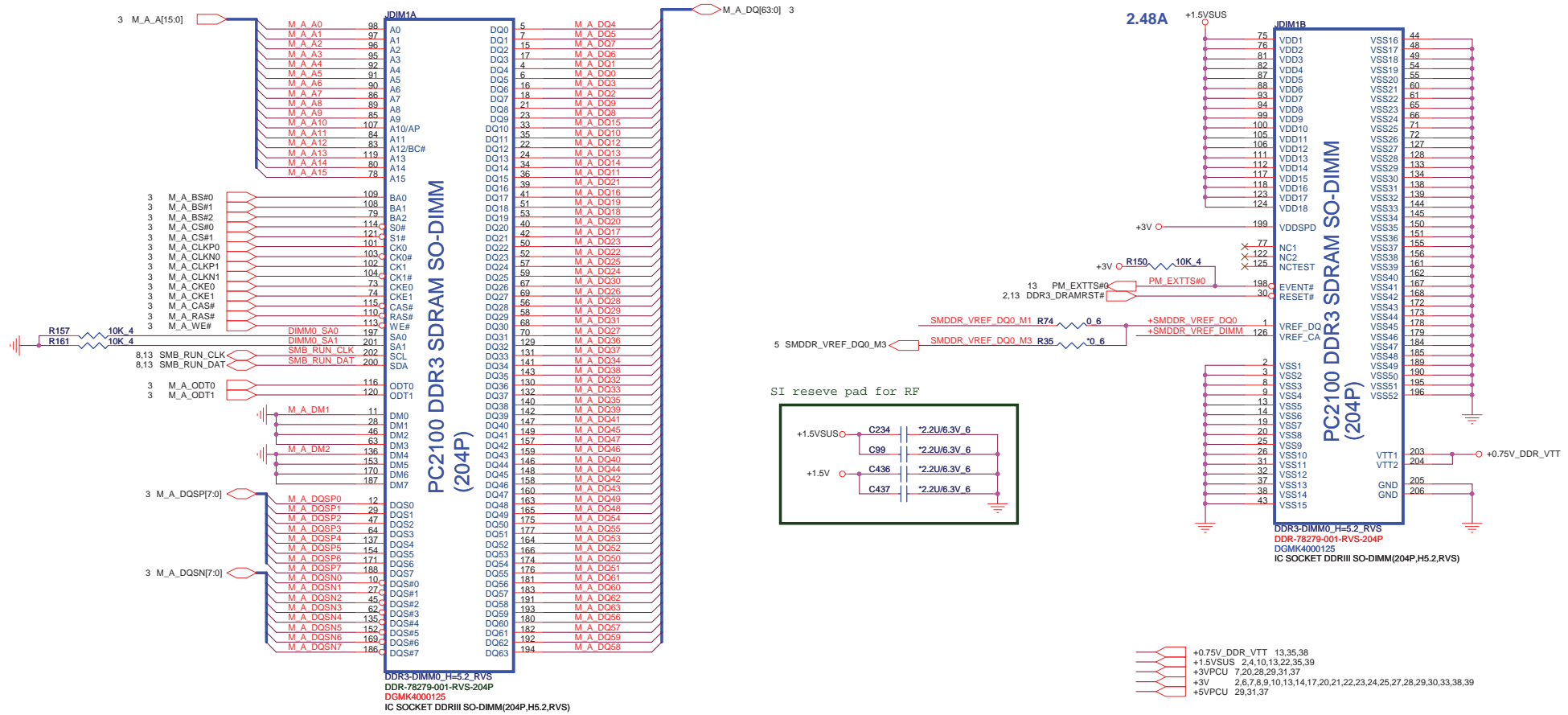


IBEX PEAK-M (GND)



IBEX PEAK-M (GND)





VREF DQ0 M2 Solution

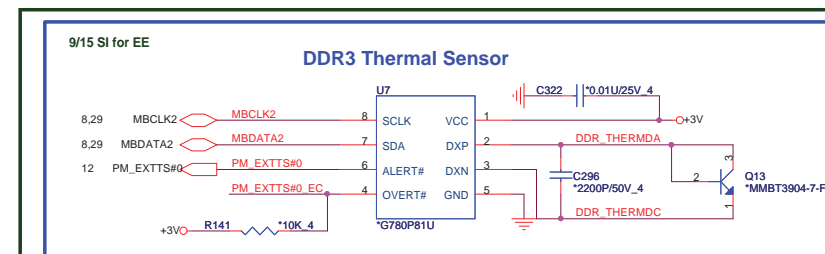
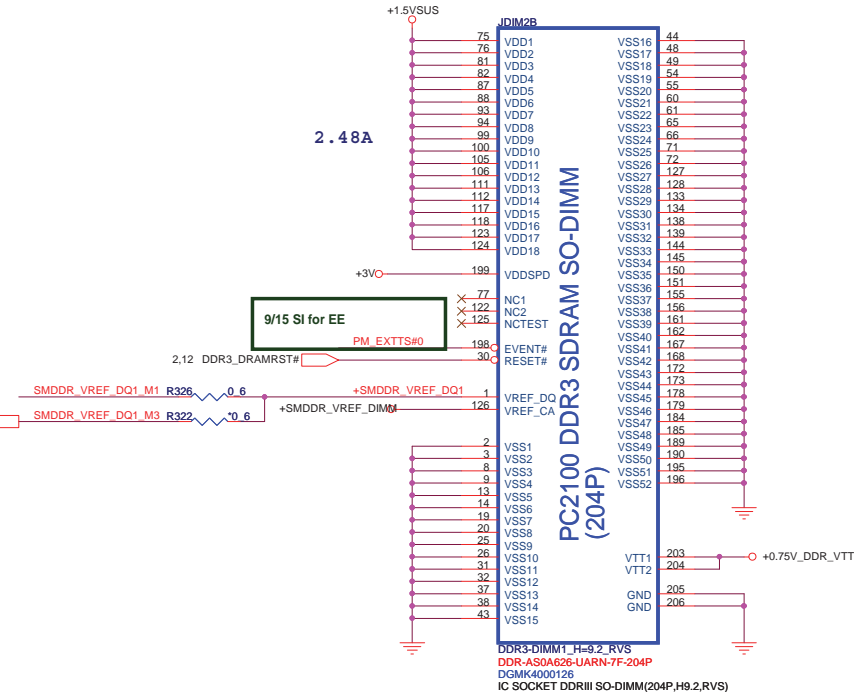
Place these Caps near So-Dimm0.

VREF DQ0 M1 Solution

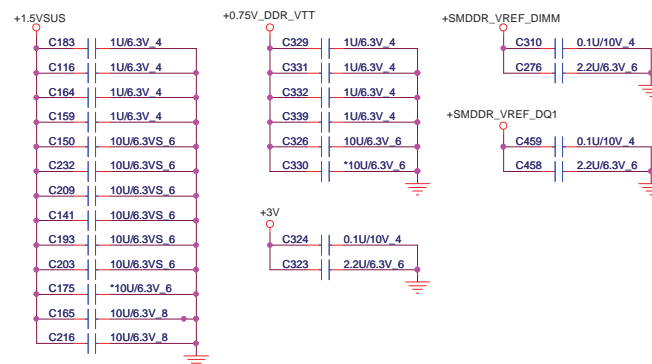


PROJECT : R13
Quanta Computer Inc.

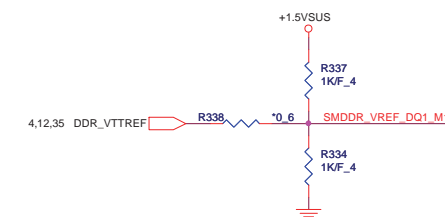
Size	Document Number	Rev
Custom	DDR3 DIMM0-RVS (5.2H)	3A
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Place these Caps near So-Dimm1.

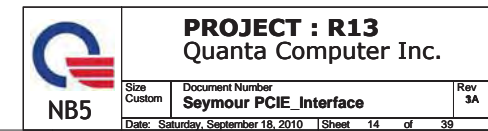
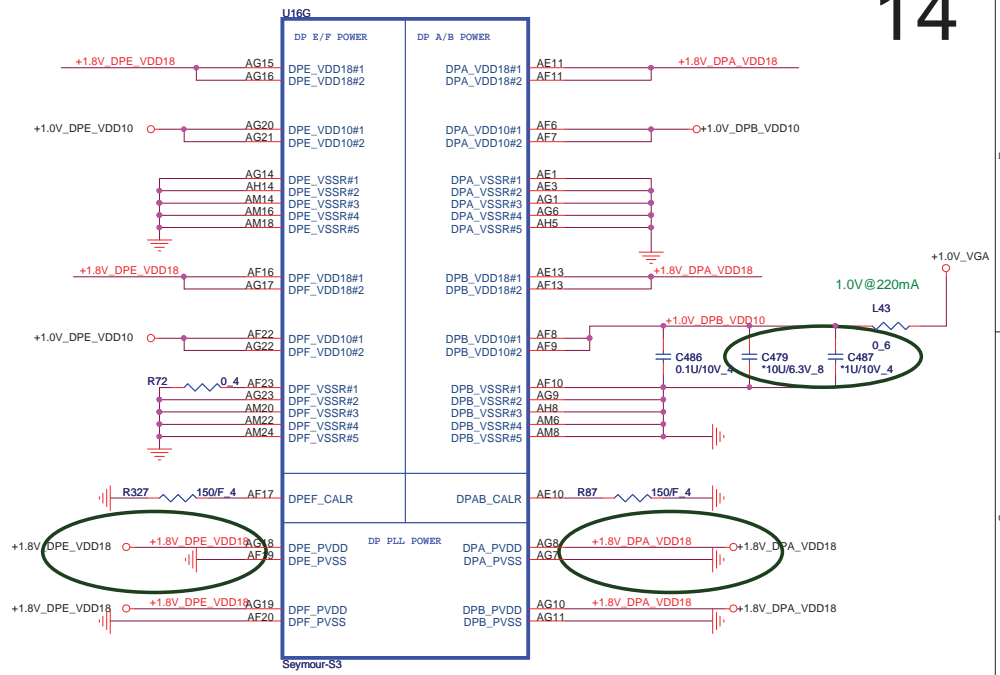


VREF DQ1 M1 Solution

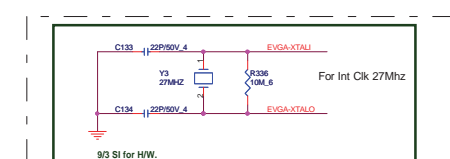
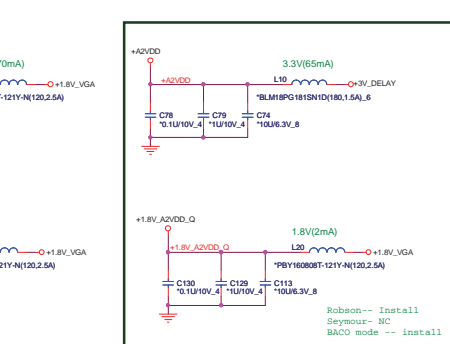
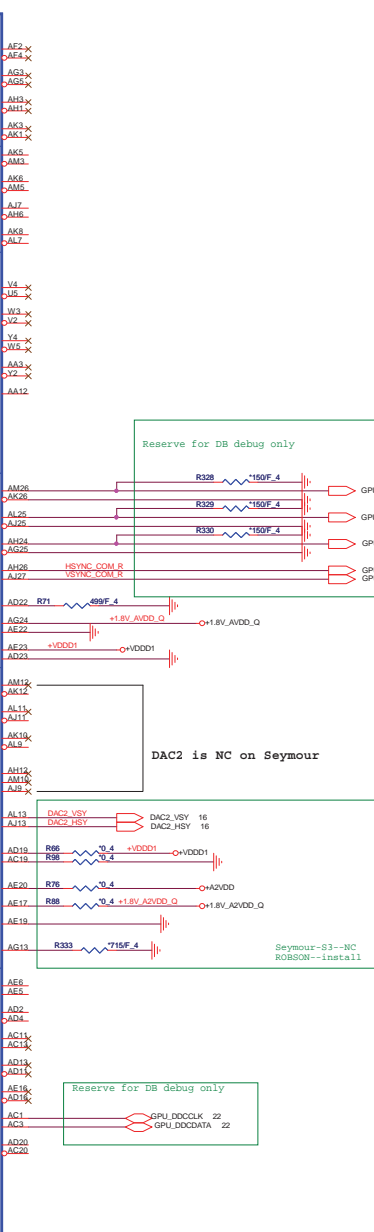
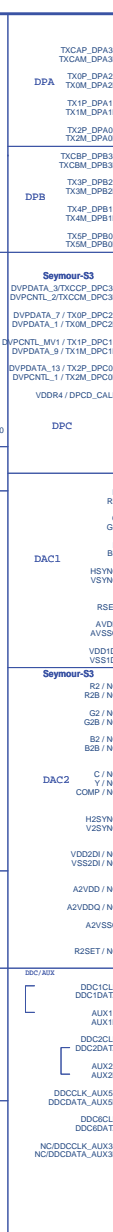
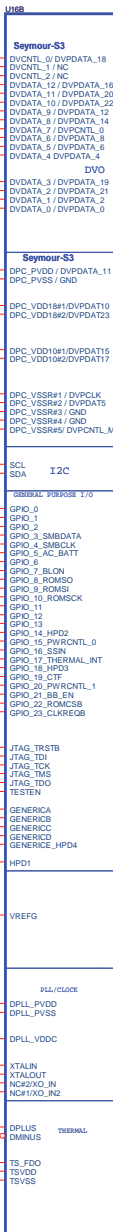
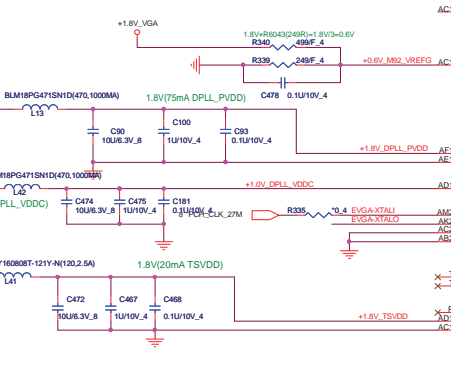
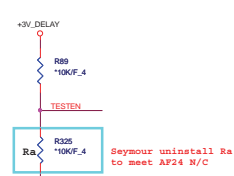


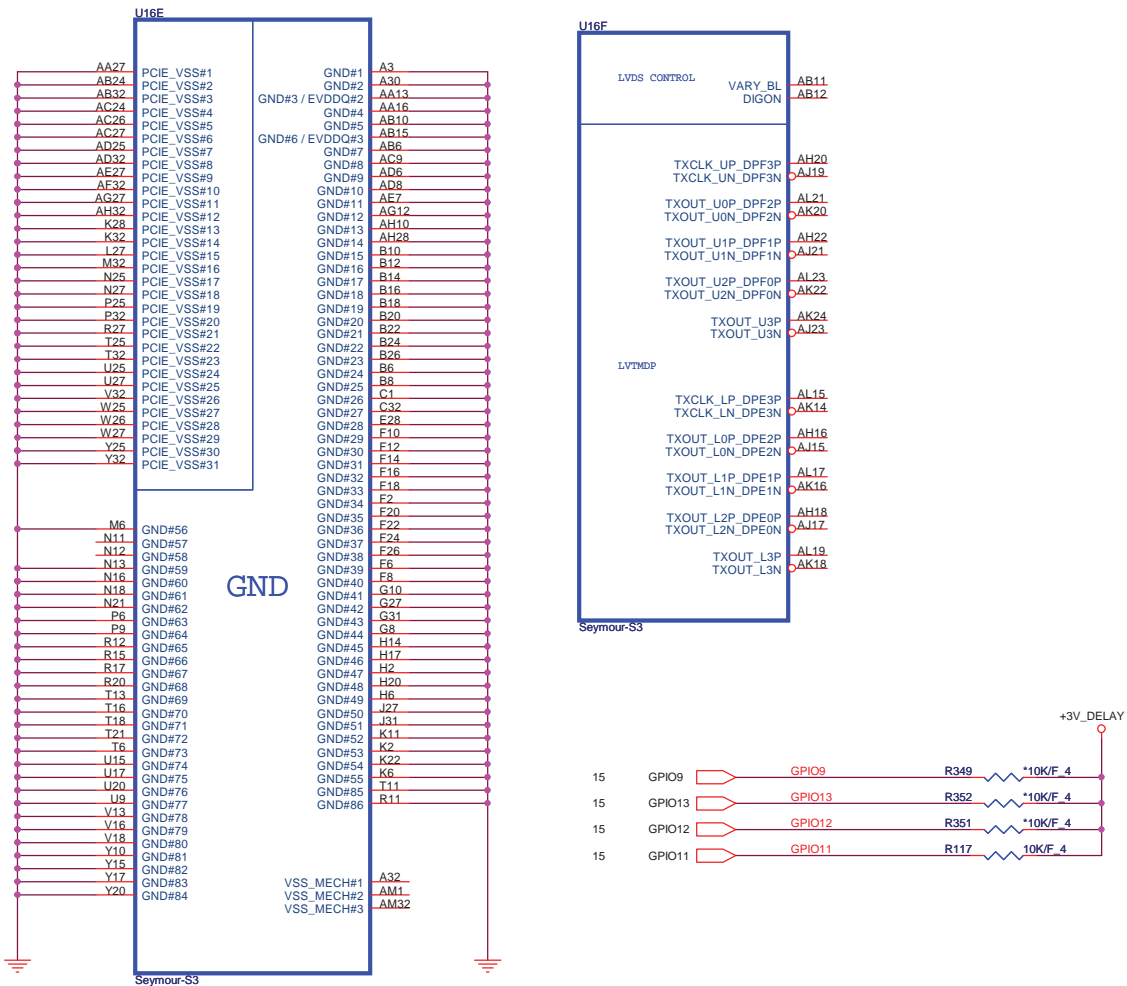
PROJECT : R13
Quanta Computer Inc.

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 3A
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Seymour	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	1V
H	1	0	1.1V (Default)
TBD	1	1	NA

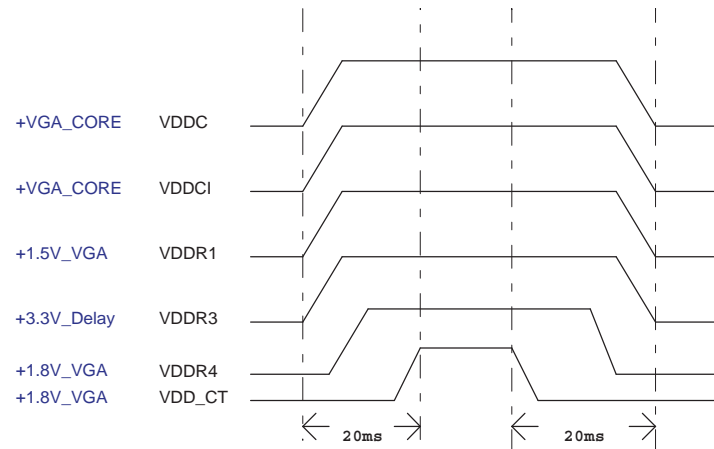




CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:1]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS		
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
H2SYNC	GENERICC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET		
GPIO21_BB_EN		

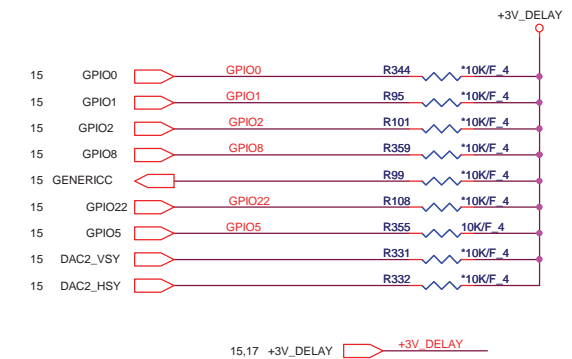
Power Up/Down Sequence



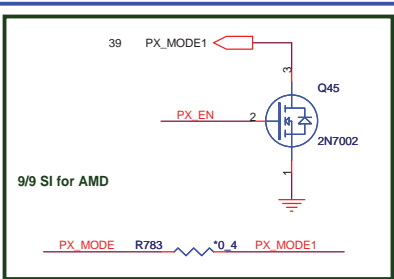
Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

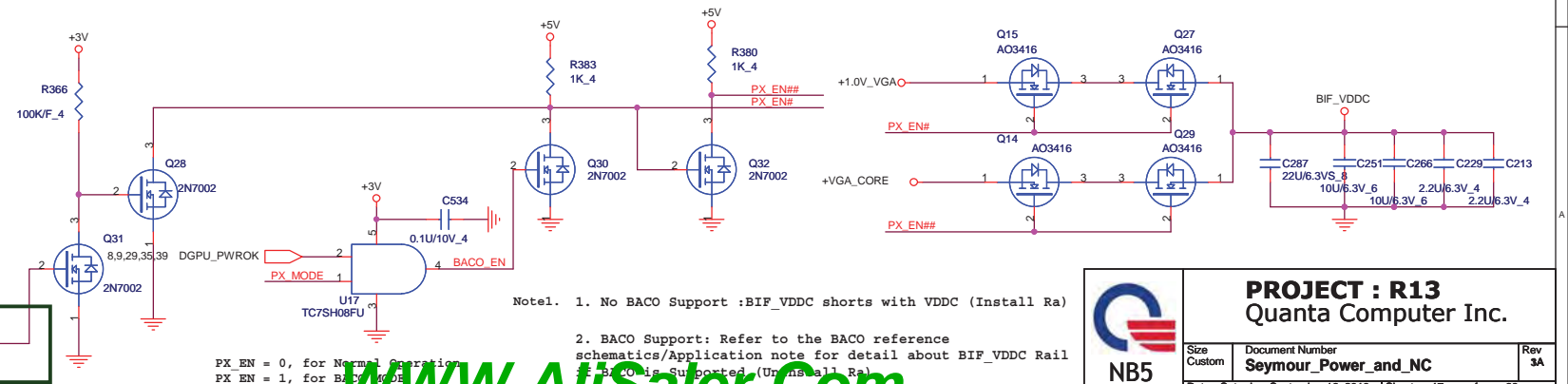
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



	PROJECT : R13 Quanta Computer Inc.		
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Support BACO Mode

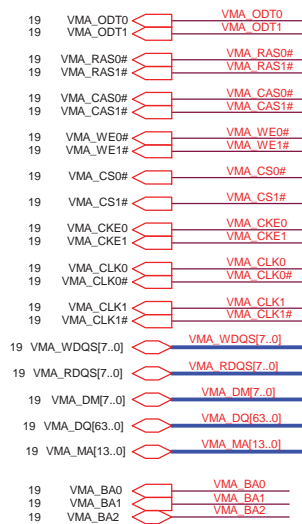


2. BACO Support: Refer to the BACO reference schematics/Application note for detail about BIF_VDDC Rail. If BACO is Supported (Unis all Rail)



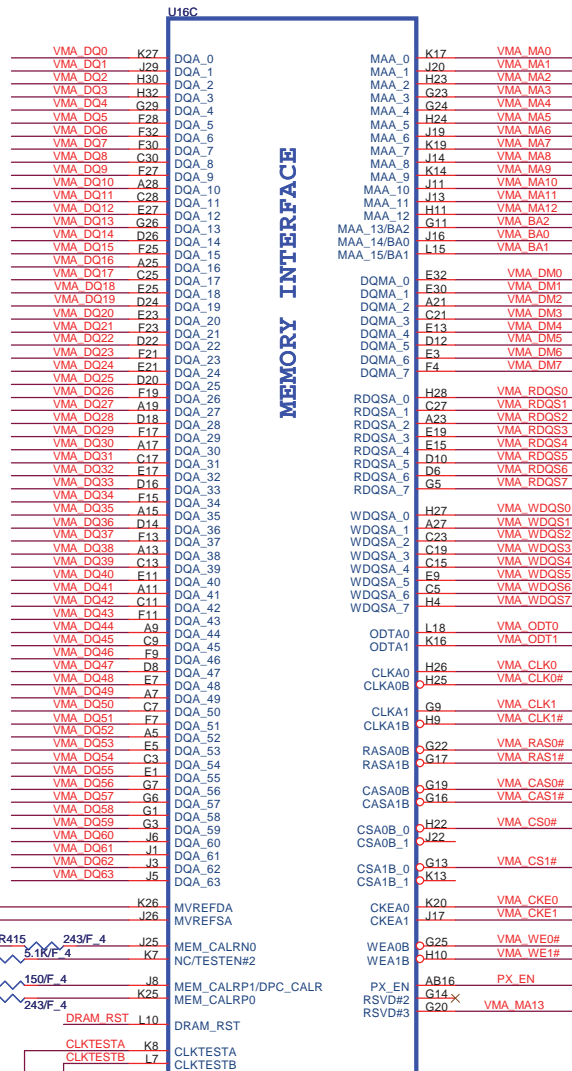
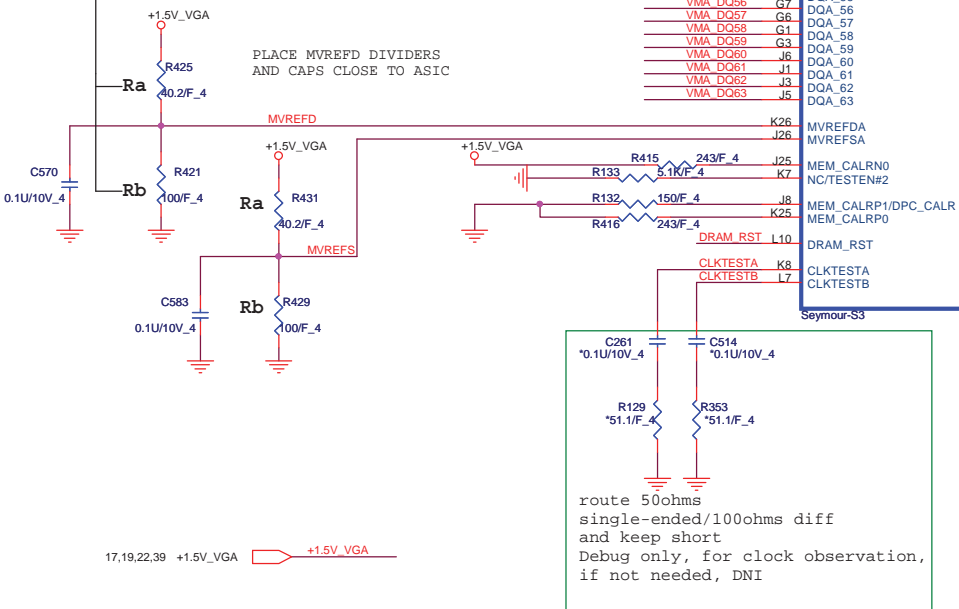
PROJECT : R13
Quanta Computer Inc.

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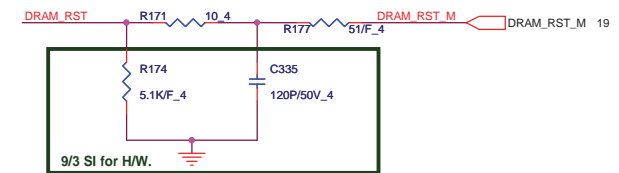


support 1Gbit
VRAM (64M X 16)

DIVIDER RESISTORS	GDDR5	DDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

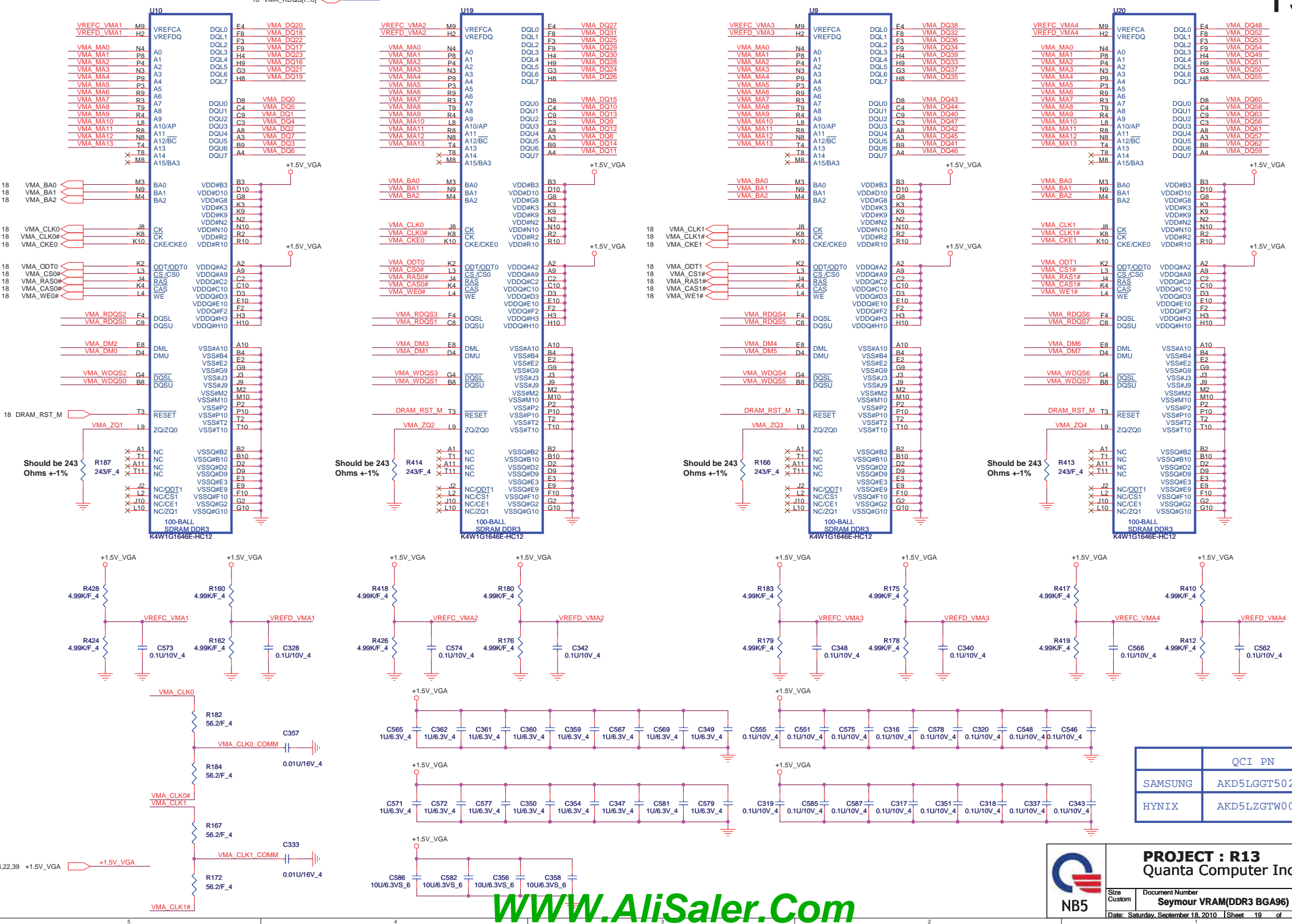


MEMORY INTERFACE



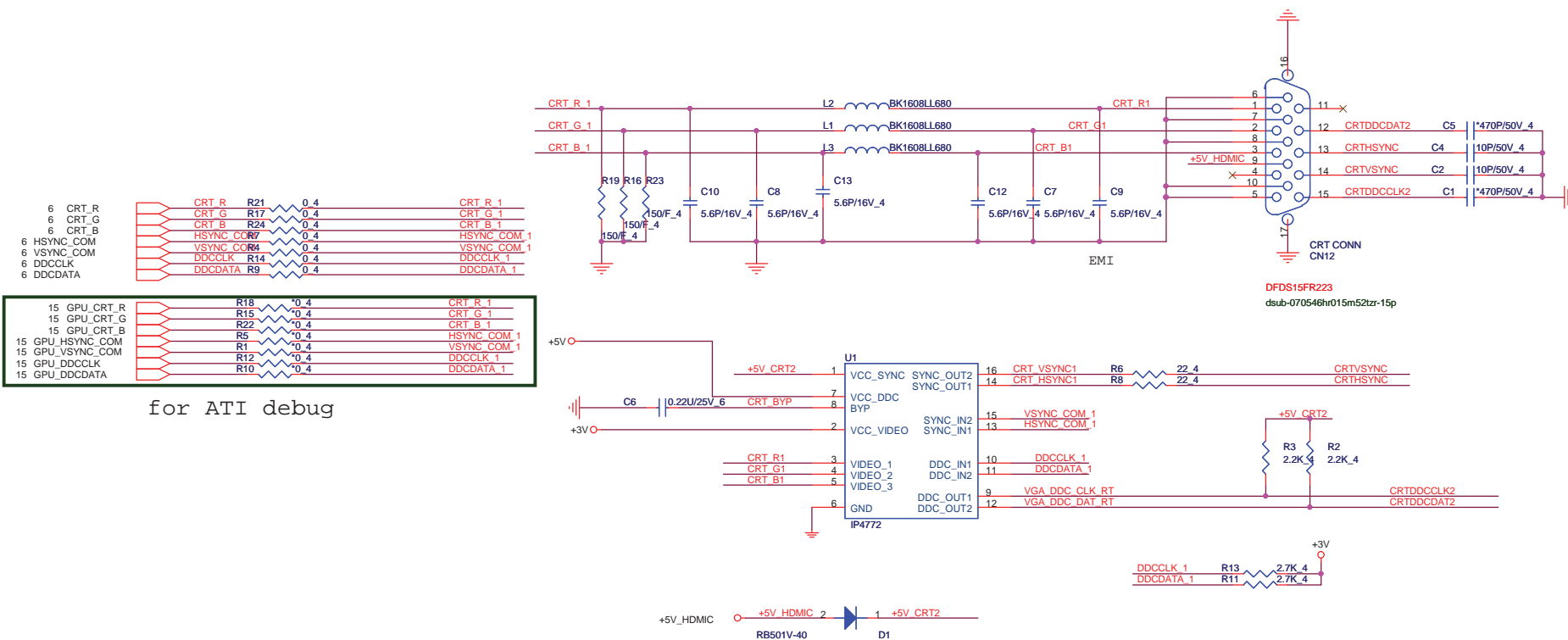
PROJECT : R13
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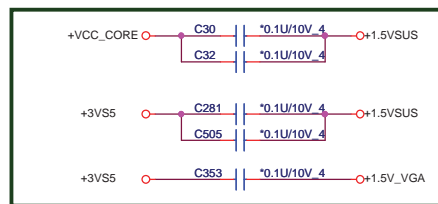
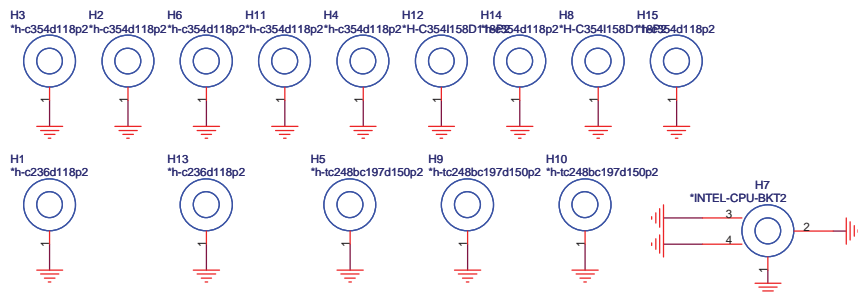




CRT PORT



HOLE



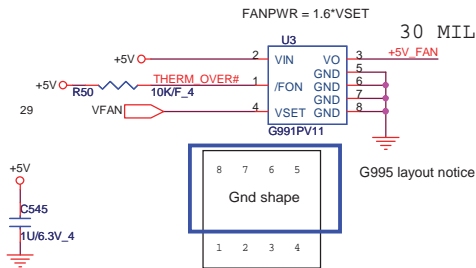
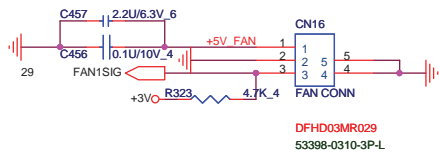
RF solution



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Quanta Computer Inc.

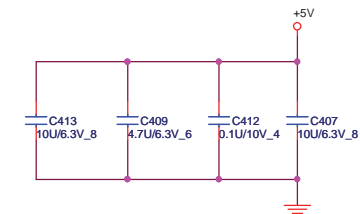
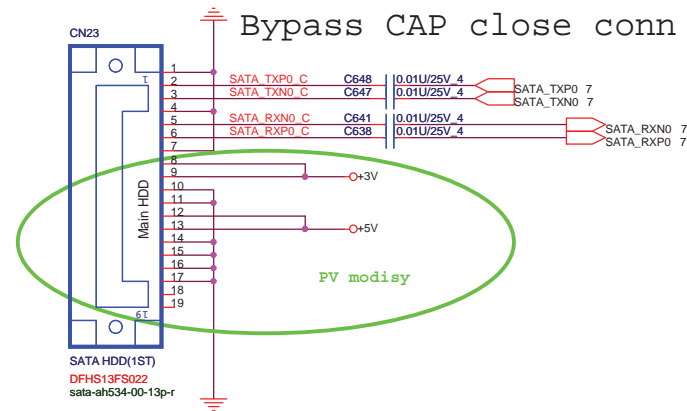
Size Custom Document Number CRT,Hole Rev 3A
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CPU FAN

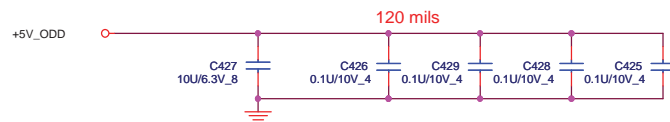
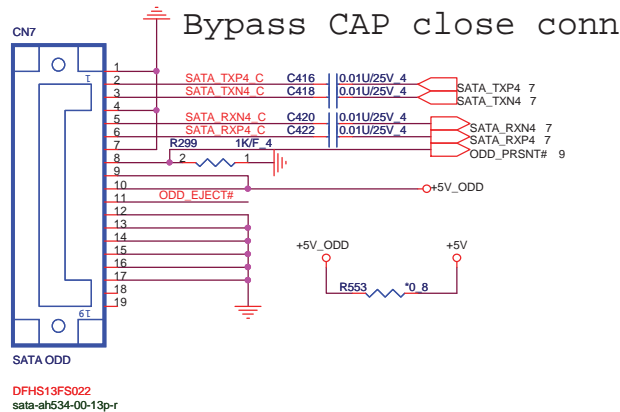


SATA HDD CONNECTOR

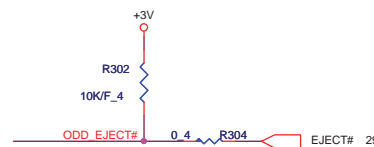
23



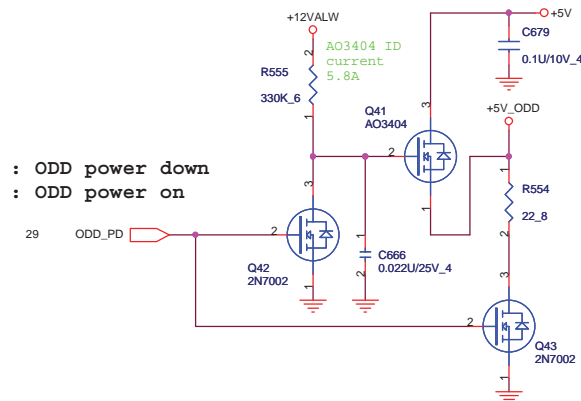
SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.

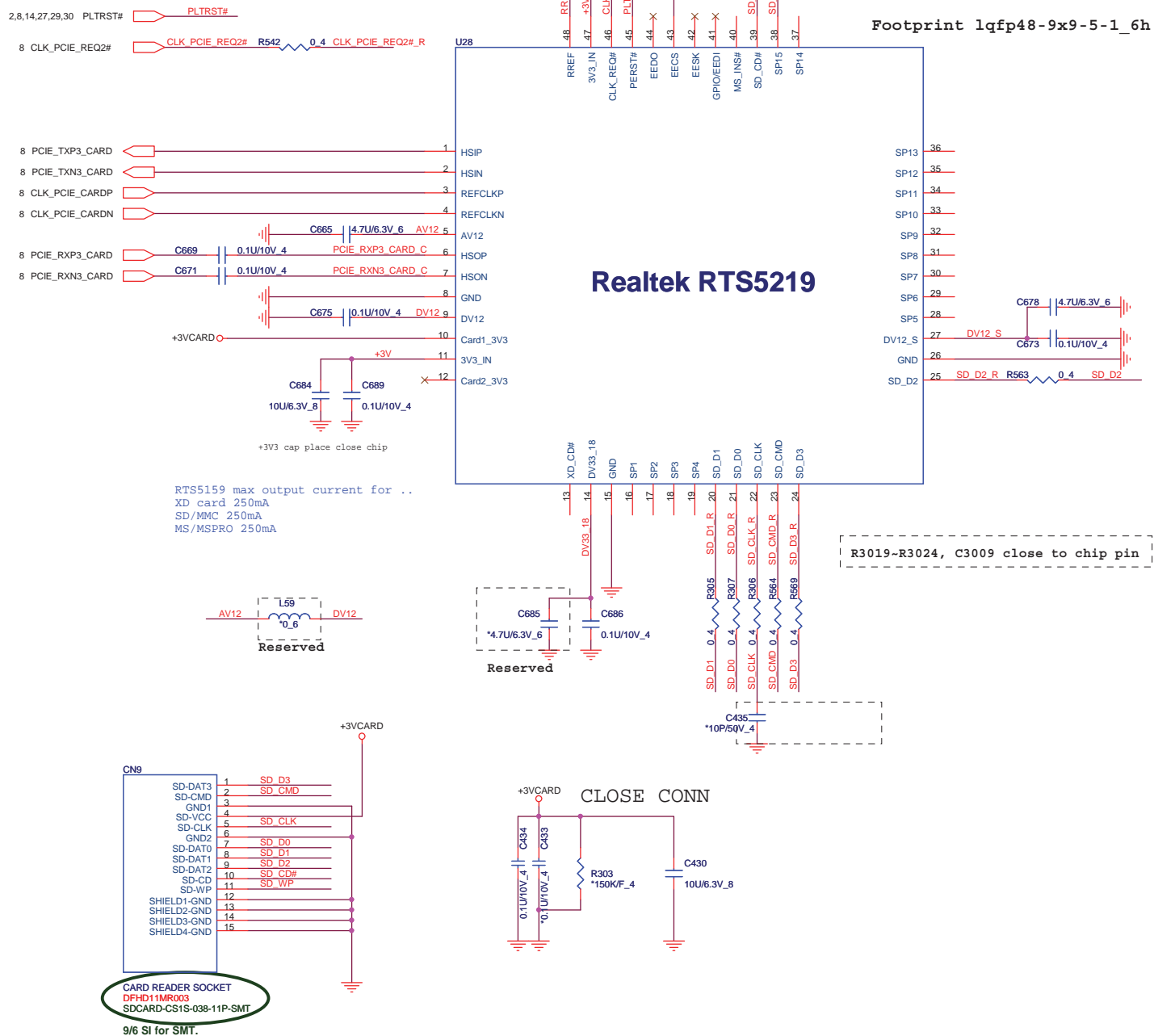


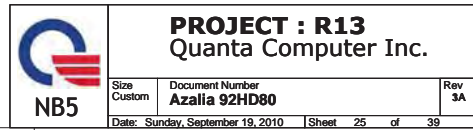
High : ODD power down
Low : ODD power on

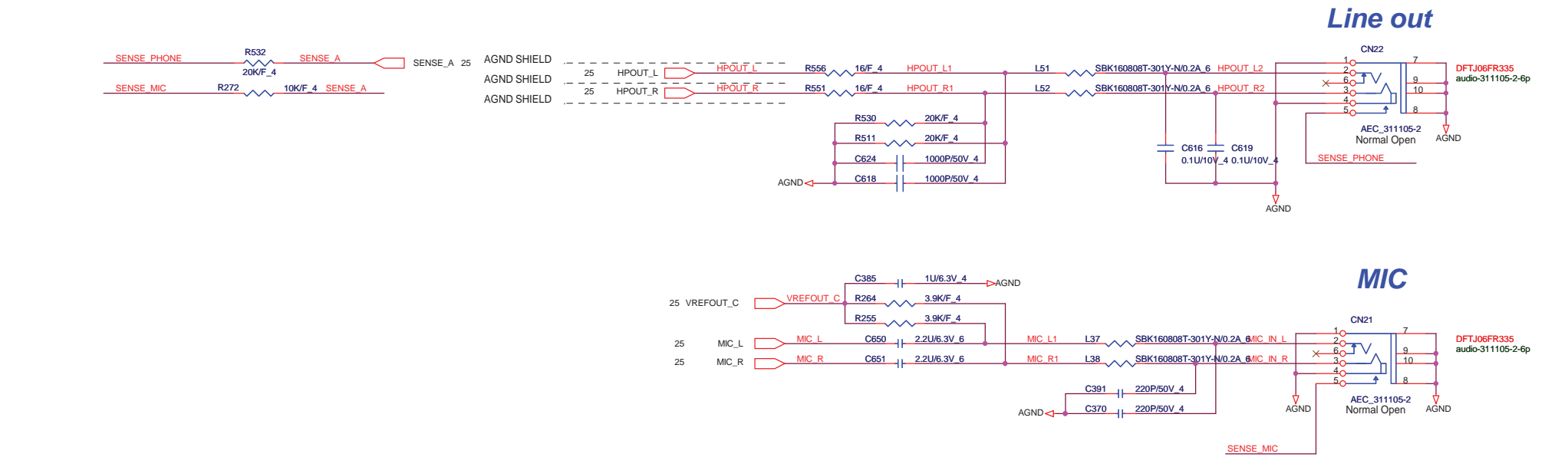
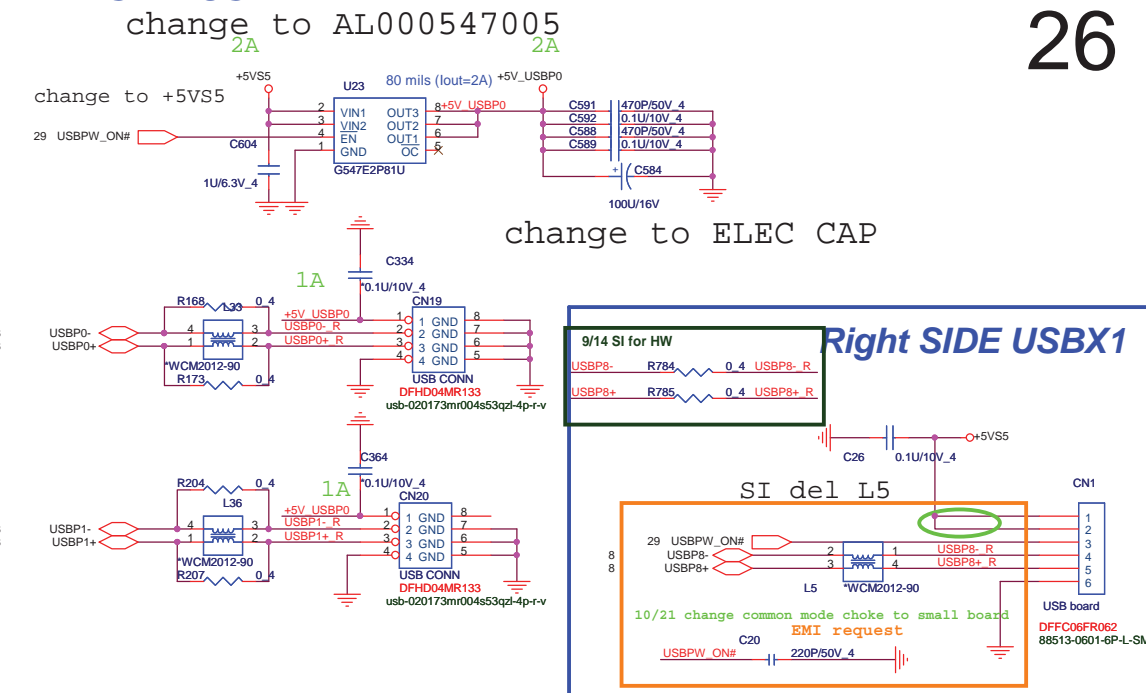
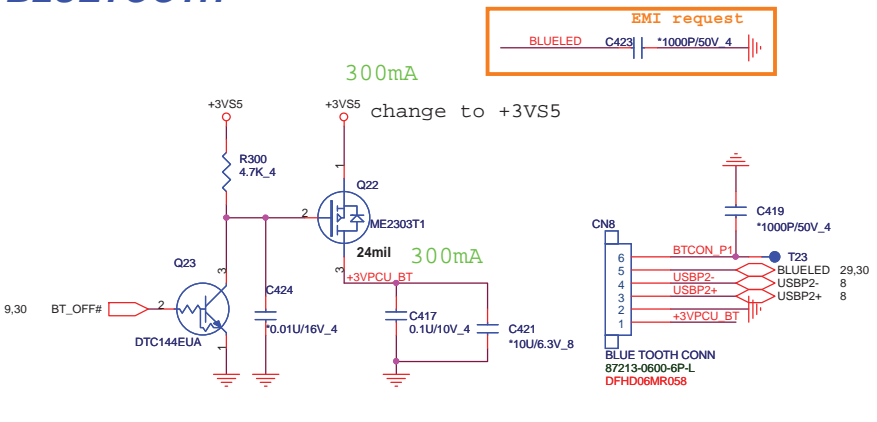


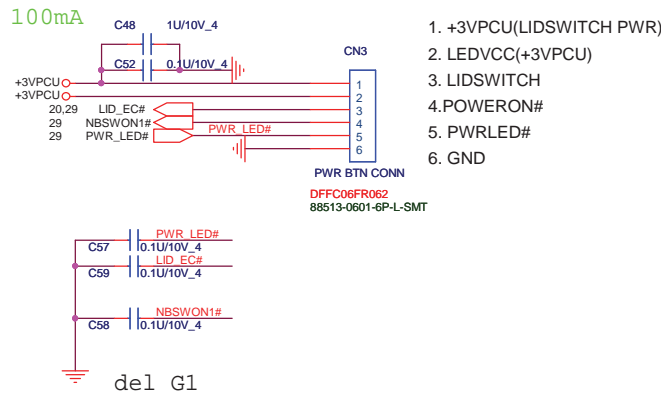
PROJECT : R13
Quanta Computer Inc.

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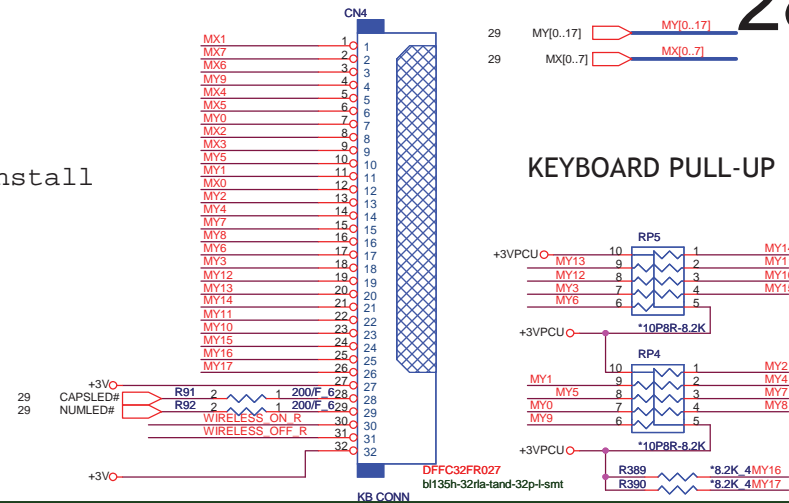




KEYBOARD Con.

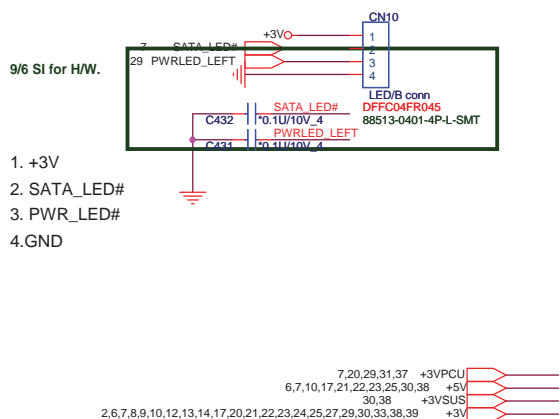


SI un-install

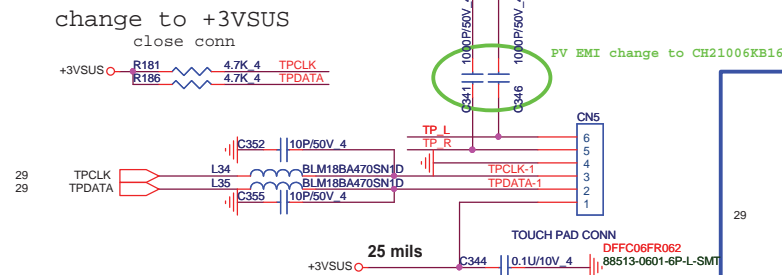


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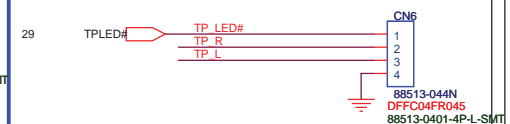
LED Con.



TOUCH PAD Con.



To TOUCH PAD SW board



adapter Type check

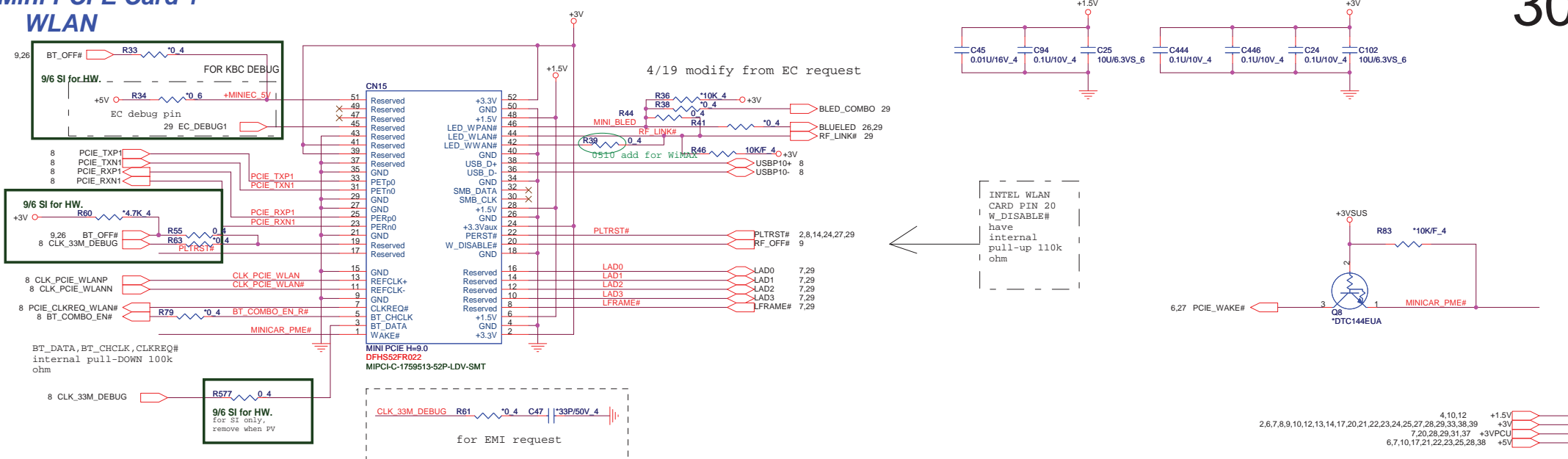
adapter select for EC

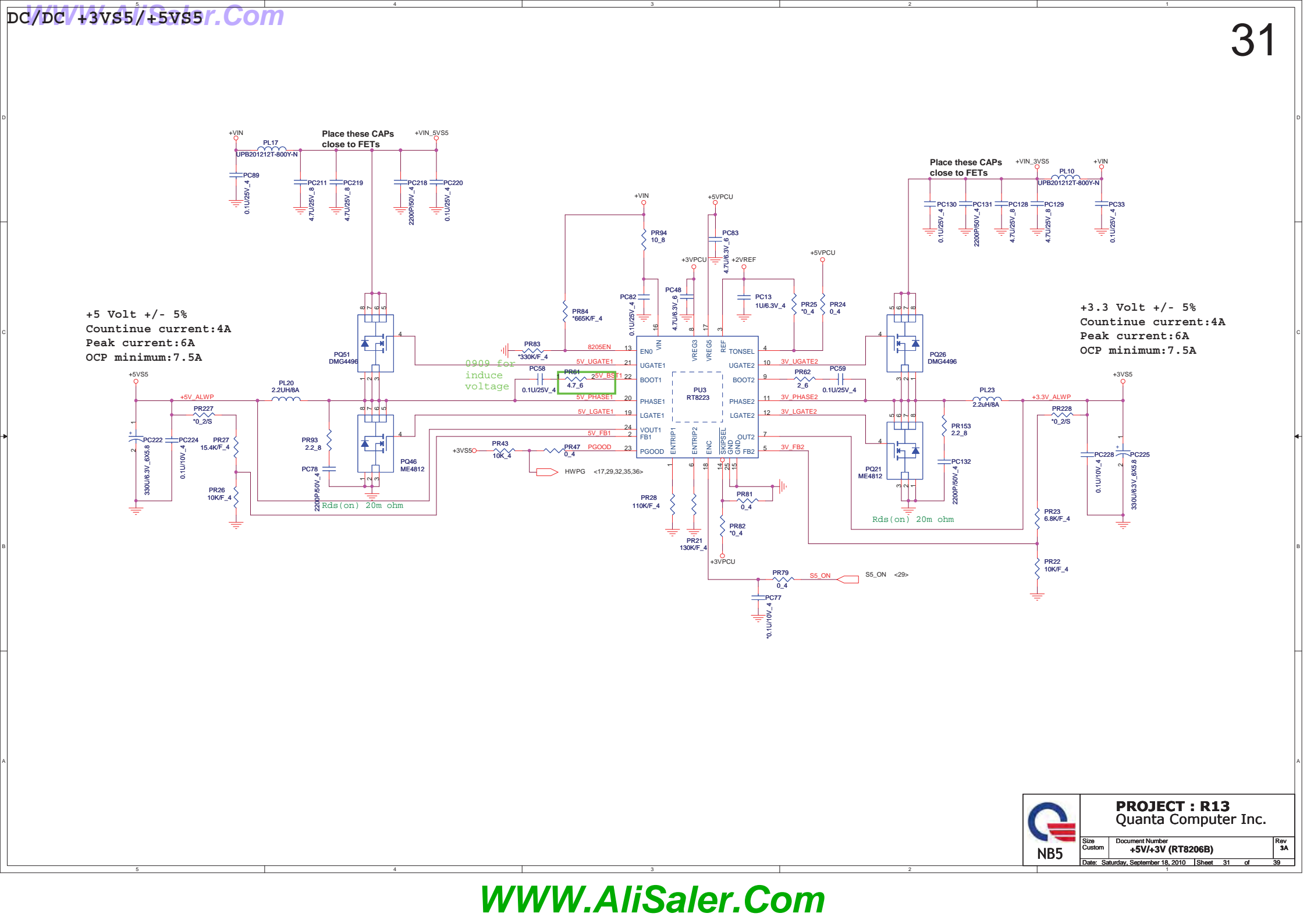
512K byte SPI EC ROM

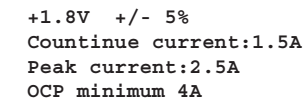
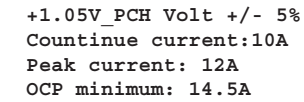
SOIC8-8-1_27

128K byte SPI EC ROM

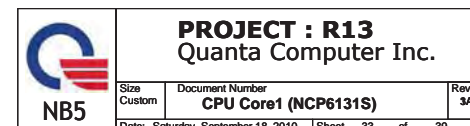
Size Custom	Document Number EC (KB3926)/ROM
Date: Saturday, September 18, 2010	Sheet 29 of 39

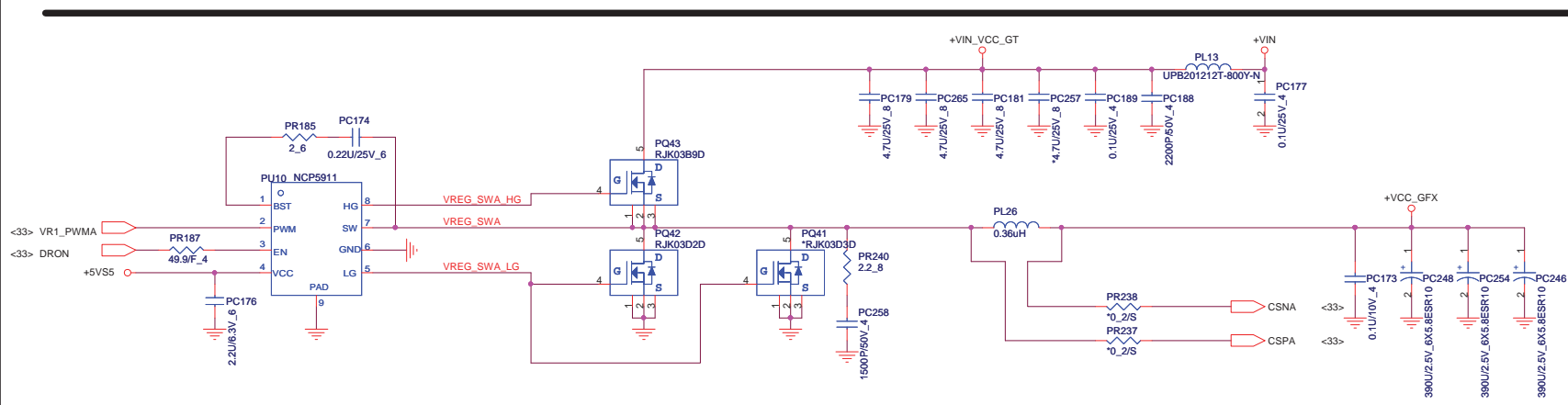





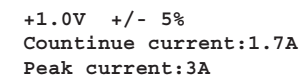
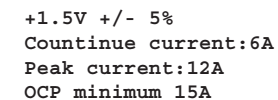


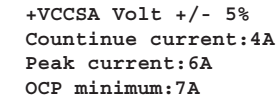
$$V_0 = 0.827 * (R_1 + R_2) / R_2$$

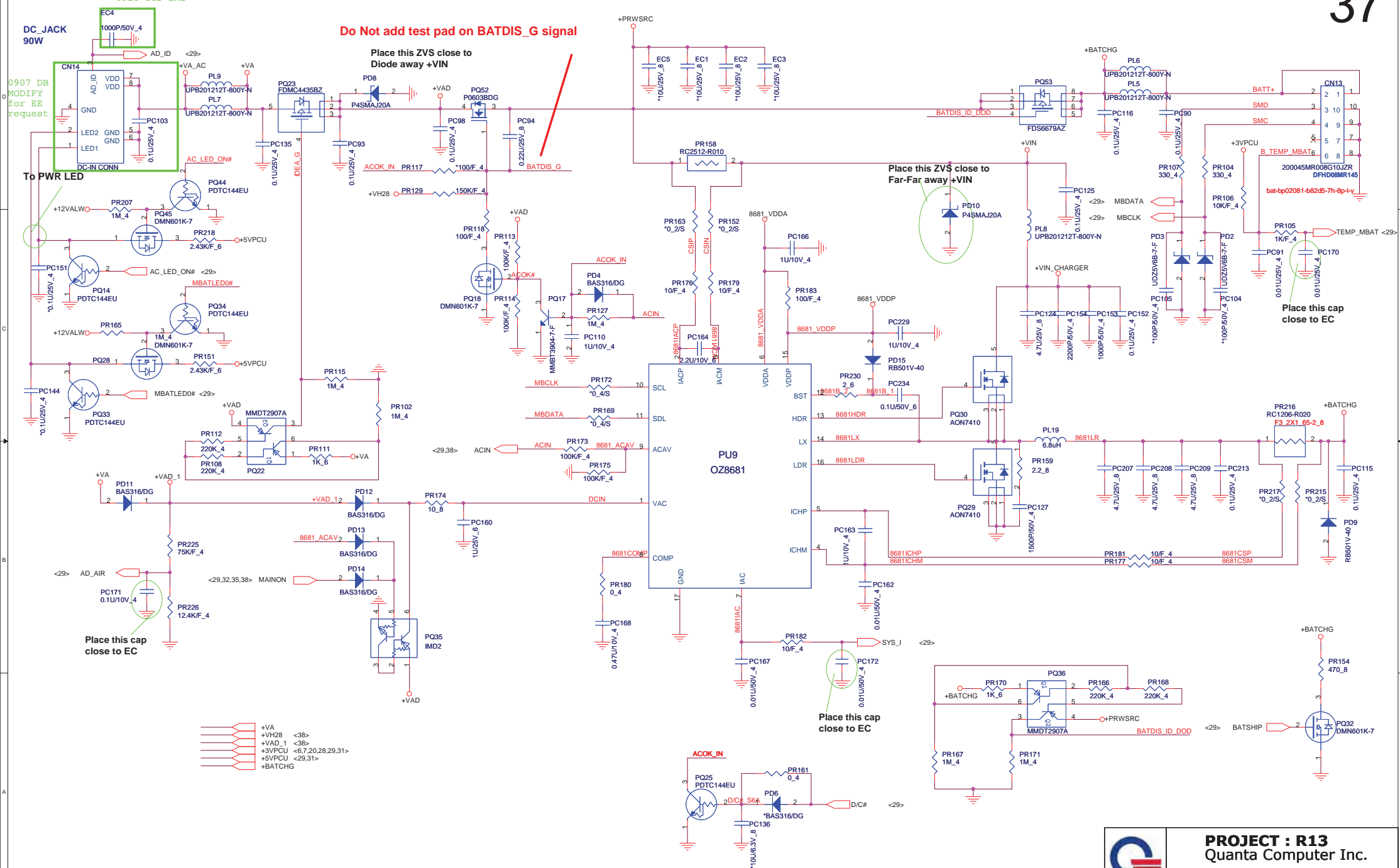


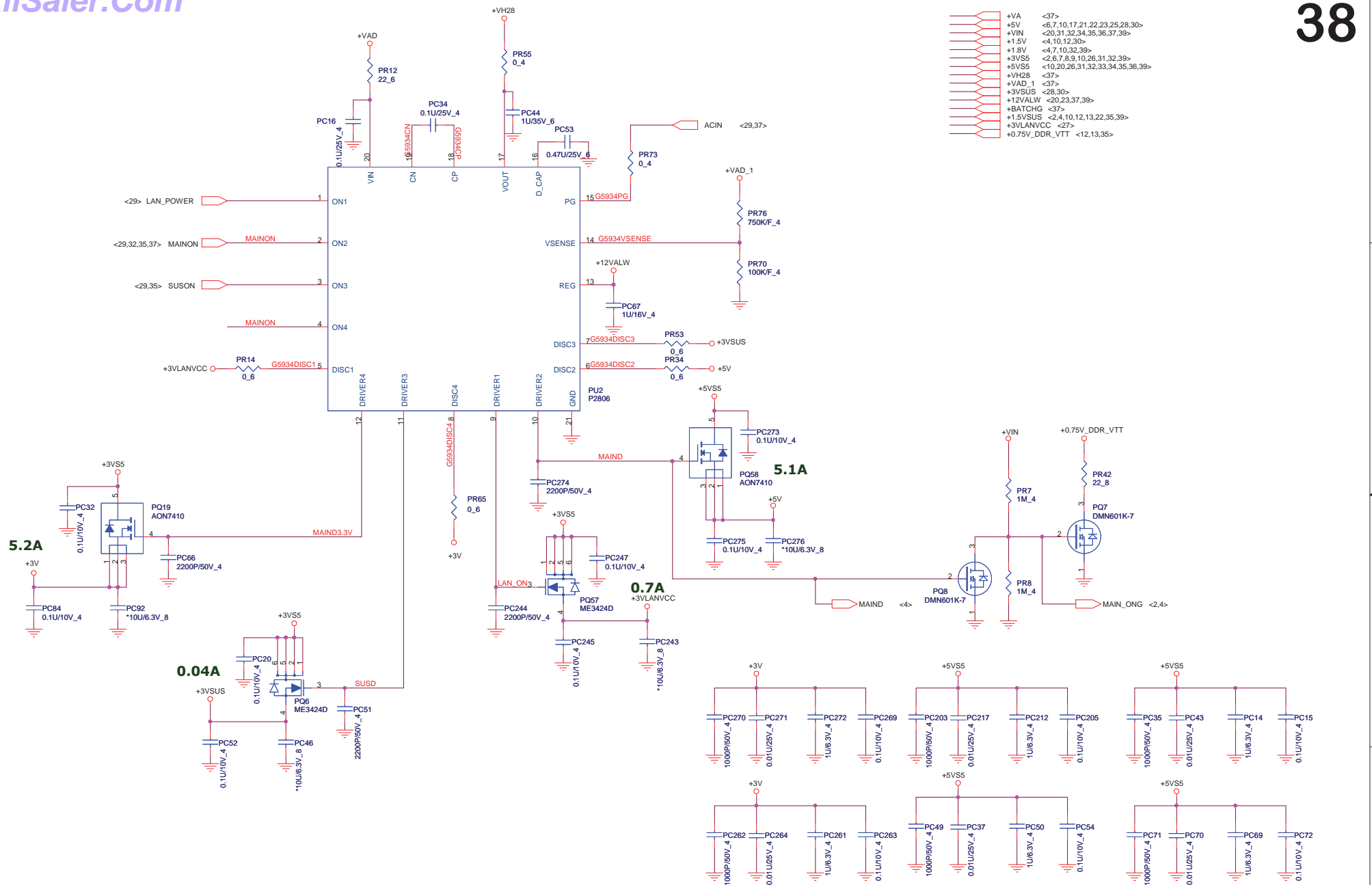


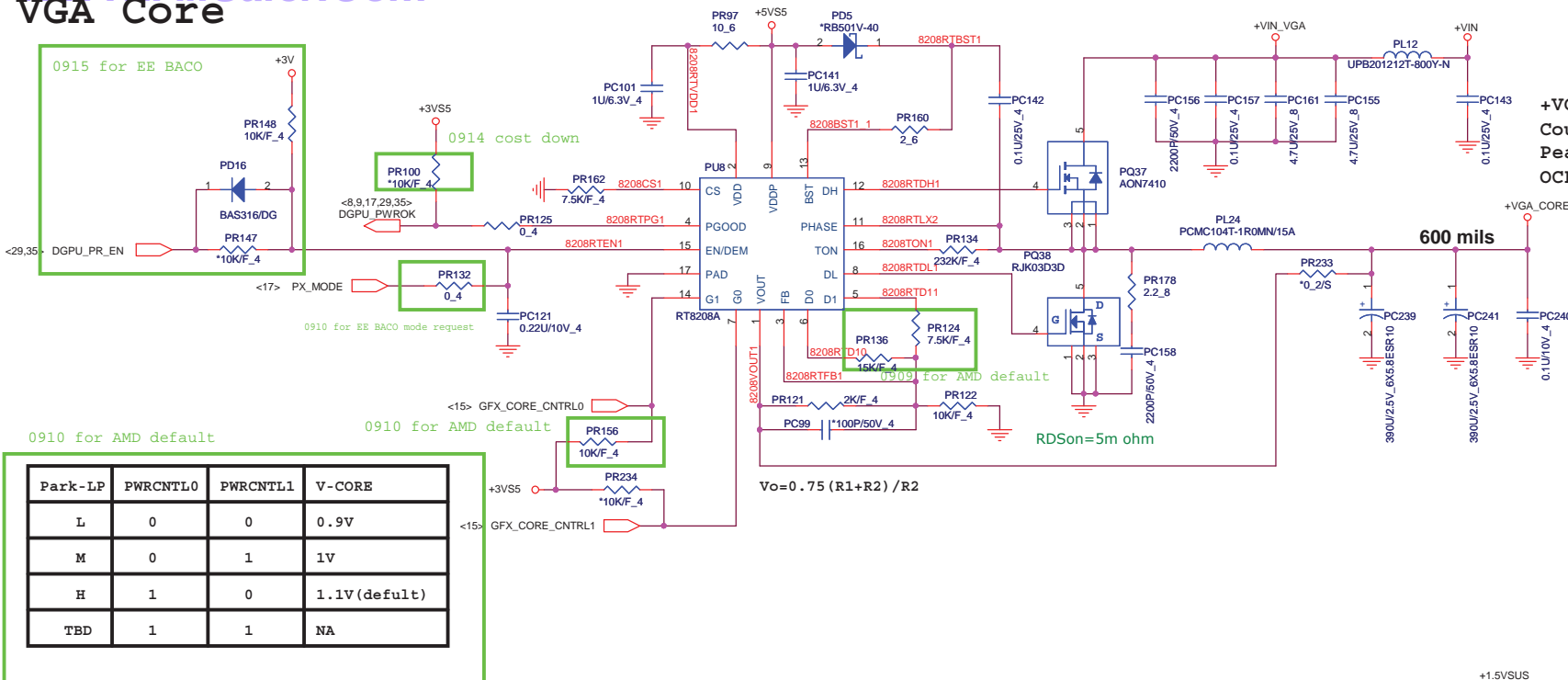
 NB5	PROJECT : R13 Quanta Computer Inc.		
	Size Custom	Document Number CPU Core2 (NCP5911)	Rev 3A
Date: Saturday September 18 2010 Sheet 34 of 39			











+VGACORE +/- 5%
 Countinue current:10A
 Peak current:14A
 OCP minimum 16A

